In the Claims

1. (Previously presented) A data slicer comprising:

a first differential comparator circuit that establishes a first threshold and that includes first and second output nodes having respective first and second polarities;

a second differential comparator circuit that establishes a second threshold and that includes first and second output nodes having respective first and second polarities; and

a third differential comparator circuit that establishes a third threshold and that includes first and second output nodes having respective first and second polarities;

wherein the second threshold is greater than the first threshold and less than the third threshold,

wherein each of the differential comparator circuits has an offset,

wherein the first and third differential comparator circuits have symmetrical offsets, and

wherein the first output node of the first differential comparator is coupled to the second output node of the third differential comparator.

2. (Currently amended) The data slicer of claim 1 wherein:

each of the differential comparator circuits includes first and second branches coupled to the respective first and second output nodes;

the first branch of the first differential comparator includes a first impedance element coupled to the first output node and a second impedance element coupled to the first impedance element at an offset node;

the second branch of the third differential comparator includes a first impedance element coupled to the second output node and a second impedance element coupled to the

first impedance element at an offset node; and

the ~~offest~~ offset node of the first differential comparator is coupled to the ~~offfset~~ offset node of the third differential comparator.

3. (Previously presented) A data slicer comprising:

a first comparator circuit that establishes a first threshold;

a second comparator circuit that establishes a second threshold; and

a third comparator circuit that establishes a third threshold;

wherein the second threshold is greater than the first threshold and less than the third threshold,

wherein each of the comparator circuits has an offset,

wherein the first and third comparator circuits have symmetrical offsets, and

wherein each of the first and third comparator circuits includes a load resistor having a center tap and wherein the load resistor center tap of the first comparator circuit is coupled to the load resistor center tap of the third comparator circuit to provide the first and second comparator circuits with symmetrical offsets.

4. (Original) The data slicer of claim 1 wherein the first and third thresholds are equally spaced from the second threshold.

5. (Previously presented) The data slicer of claim 1 wherein the differential comparator circuits are formed from complimentary metal oxide semiconductor devices.

6. (Previously presented) A data slicer comprising:

a first differential comparator circuit that establishes

a first threshold and that includes first and second output nodes having respective first and second polarities and an output circuit coupled to the first output node;

a second differential comparator circuit that establishes a second threshold and that includes first and second output nodes having respective first and second polarities and an output circuit coupled to the first output node; and

a third differential comparator circuit that establishes a third threshold and that includes first and second output nodes having respective first and second polarities and an output circuit coupled to the first output node;

wherein the second threshold is greater than the first threshold and less than the third threshold,

wherein each of the differential comparator circuits has an offset,

wherein the first and third differential comparator circuits have output circuits providing symmetrical offsets, and

wherein the output circuit of the first differential comparator is coupled to the output circuit of the third differential comparator.

7. (Previously presented) A data slicer comprising:

a first comparator circuit that establishes a first threshold;

a second comparator circuit that establishes a second threshold; and

a third comparator circuit that establishes a third threshold;

wherein the second threshold is greater than the first threshold and less than the third threshold;

wherein each of the comparator circuits has an offset,

wherein the first and third comparator circuits have

output circuits providing symmetrical offsets, and

wherein the output circuit of each of the first and third comparator circuits includes a load resistor having a center tap and wherein the load resistor center tap of the first comparator circuit is coupled to the load resistor center tap of the third comparator circuit to provide the first and second comparator circuits with the symmetrical offsets.

8. (original) The data slicer of claim 6 wherein the first and third thresholds are equally spaced from the second threshold.

9. (Previously presented) The data slicer of claim 6 wherein the differential comparator circuits are formed from complimentary metal oxide semiconductor devices.

10. (Currently amended) A data slicer comprising:

a first comparator circuit that establishes a first threshold;

a second comparator circuit that establishes a second threshold; and

a third comparator circuit that establishes a third threshold,

wherein the second threshold is greater than the first threshold and less than the third threshold,

said first comparator circuit comprising a first load resistor having a first center tap,

said second comparator circuit comprising a second load resistor having a second center tap, wherein said first center tap is coupled to said second center tap,

~~wherein the first and third comparator circuits each includes a load resistor having a center tap, and~~

~~wherein the load resistor center tap of the first~~

~~comparator circuit is coupled to the load resistor center tap of the third comparator circuit~~.

11. (original) The data slicer of claim 10 wherein the first and third thresholds are equally spaced from the second threshold.

12. (original) The data slicer of claim 10 wherein the comparator circuits are formed from complimentary metal oxide semiconductor devices.

13. (Previously presented) An integrated circuit comprising:

a substrate of semiconductor material; and

a data slicer formed in the semiconductor material, the data slicer including,

a first differential comparator circuit that establishes a first threshold and that includes first and second output nodes having respective first and second polarities,

a second differential comparator circuit that establishes a second threshold and that includes first and second output nodes having respective first and second polarities, and

a third differential comparator circuit that establishes a third threshold and that includes first and second output nodes having respective first and second polarities,

wherein the second threshold is greater than the first threshold and less than the third threshold,

wherein each of the differential comparator circuits has an offset,

wherein the first and third differential comparator circuits have symmetrical offsets, and

wherein the first output node of the first differential comparator is coupled to the second output node of the third differential comparator.

14. (Previously presented) The integrated circuit of claim 13 wherein the first and third differential comparator circuits have output circuits providing the symmetrical offsets.

15. (Previously presented) An integrated circuit comprising:

a substrate of semiconductor material; and

a data slicer formed in the semiconductor material, the data slicer including,

a first comparator circuit that establishes a first threshold,

a second comparator circuit that establishes a second threshold, and

a third comparator circuit that establishes a third threshold,

wherein the second threshold is greater than the first threshold and less than the third threshold,

wherein each of the comparator circuits has an offset,

wherein the first and third comparator circuits have symmetrical offsets, and

wherein each of the first and third comparator circuits includes a load resistor having a center tap and wherein the load resistor center tap of the first comparator circuit is coupled to the load resistor center tap of the third comparator circuit to provide the first and second comparator circuits with symmetrical offsets.

16. (original) The integrated circuit of claim 13 wherein the first and third thresholds of the data slicer are equally spaced from the second threshold.

17. (Previously presented) The integrated circuit of claim 13 wherein the differential comparator circuits are formed from complimentary metal oxide semiconductor devices.

18. (Previously presented) The data slicer of claim 2 wherein each impedance element comprises a resistor.